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E Waingold, M Taylor, V Sarkar, W Lee, V Lee, J ... - IEEE Computer, 1997 - aar.cs.ucdavis.edu
... The onerous compile times of our **multi-FPGA** based Raw prototype computer (see Section 6 ... The processor/**network interface** is shared between the two networks. ...
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[PS] The Transmogrifier: The University of Toronto Field-Programmable System
D Galloway, D Karchmer, P Chow, D Lewis, J Rose - Second Canadian Workshop on Field-Programmable Devices, ..., 1994 - eecg.toronto.edu
... **Interface** Board ... 4. TM-1 Interconnection **Network** In typical **multi-FPGA** boards, eg [Gokhale91], the wires that connect the FPGAs together are usually hard-wired ...
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Logic Partition Orderings for **Multi-FPGA** Systems - group of 10 »
S Hauck, G Borriello - FPGA, 1995 - doi.ieeecomputersociety.org
... Logic Partition Orderings for **Multi-FPGA** Systems ... This allows **multi-FPGA** partitioners to harness standard partitioning techniques. ...
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A hardware implementation of a signaling protocol - group of 5 »
H Wang, M Veeraraghavan, R Karri - Proc. of Opticomm 2002 - ece.virginia.edu
... is that an out-of-band IP **network** will be ... timeslot pair and the outgoing **interface**/timeslot pair ... We used the WILDFORCE TM **multi-FPGA** reconfigurable computing ...
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Scalable Pattern Matching for High Speed Networks - group of 6 »
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... devices such as routers, switches, and **network interface** cards. At the upper end of the application spectrum, we envision larger, **multi- FPGA** systems operating ...
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D Roggen, S Hofmann, Y Thoma, D Floreano - Proc. 2003 NASA/DOD Conference on Evolvable Hardware, July, 2003 - doi.ieeecomputersociety.org
... I/O for the Khepera bus or user I/O • Stackable modules (**multi-FPGA** system sharing a ... UART and I/O) 2121 17.9ns • **Network interface** 163 7.83ns • Net. ...
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[PS] Interconnect Synthesis for Reconfigurable **Multi-FPGA** Architectures - group of 7 »
V Srinivasan, S Radhakrishnan, R Vemuri, J Walrath - bdd (Binary Decision Diagram) - ececs.uc.edu
... pipelined routing algorithm for **multi-FPGA** systems. ... through an api (Application Procedural **Interface**). ... that makes the interconnection **network** implement the ...
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Implementation of BEE: a real-time large-scale hardware emulation engine - group of 7 »
C Chang, K Kuusilinna, B Richards, RW Brodersen - FPGA, 2003 - portal.acm.org
... Figure 3: Various **multi-FPGA** interconnect topologies In light of the above two

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Authors Abdel Ejnioui School of Electrical Engineering and Computer Science, University of Central Florida, Orlando, FL
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